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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/380,994	09/13/1999	MASARU TAKADA	P23128USA	3373

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EXAMINER	
NORRIS, JEREMY C	
ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 06/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/380,994	TAKADA ET AL.	
	Examiner	Art Unit	
	Jeremy C. Norris	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,7,10,15 and 18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,7,10,15 and 18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/29/04,1/22/02,*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after an Office action under *Ex Parte Quayle*, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on 29 November 2004 has been entered.

Allowable Subject Matter

The indicated allowability of claims 1-4, 7, 10, 15, and 18 is withdrawn in view of the newly discovered references. Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 3 and 7 are rejected under 35 U.S.C. 102(e) as being anticipated by US 5,744,758 (Takenouchi).

Takenouchi discloses, referring primarily to figure 10, a method of manufacturing a printed wiring board having an odd number (n=3) of conductive layers (22) which are built up with a same odd number of insulating layers (12) respectively and are electrically connected to one another by first interconnecting through holes (20), the method comprising the steps of interposing the insulating layers between a second to n-th conductive layers, respectively, and also forming first interconnecting through holes for electrically connecting the conductive layers to one another; laminating a first prepreg and a copper foil on a surface of the second conductive layer, and press-bonding a second prepreg on a surface of the n-th conductive layer to form a multilayer substrate having an odd number n of insulating layers (see figure 5), wherein the second to n- th conductive layers are internal layers of the multilayer substrate; etching the copper foil to form a first conductive layer (see figures 4e-f); forming second interconnecting through holes in a first insulating layer and forming connecting holes in an n-th insulating layer, respectively; forming a metal plating film (32, see col. 10, lines 30-40) for electrically connecting the first conductive layer with a second conductive layer on the walls of the second interconnecting through holes of the first insulating layer; and connecting external connecting terminals (24) to a surface of the n-th conductive layer exposed through the first connecting through holes of the n-th insulating layer [claim 3].

Similarly, Takenouchi discloses, referring primarily to figure 3, a method of manufacturing a printed wiring board having a plurality of conductive layers (22) which are built up with insulating layers (14) respectively and are electrically connected to one

another by interconnecting through holes (32), the method comprising the steps of forming conductive layers on a plurality of insulating layers respectively; laminating and press-bonding the resulting insulating layers to form a multilayer substrate (see col. 4, lines 50-55); irradiating a laser beam (9, lines 1-10) on the multilayer substrate at interconnecting through holes forming portions to define interconnecting through holes with bottoms defined by the conductive layers; covering the walls of the interconnecting through holes with metal plating films (see col. 7, lines 50-60); and fusing solder balls (24) against the interconnecting through holes and filling them with solder [claim 7].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein

were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1, 2, and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5,744,758 (Takenouchi) in view of US 5,435,877 (Ishii).

Takenouchi discloses, referring primarily to figure 3, a printed wiring board comprising an odd number (n=3) of conductive layers (22) which are built up with a same odd number of insulating layers (12) respectively and are electrically connected to one another via interconnecting through holes (20) wherein a first conductive layer on which an electronic component layer is to be mounted (the top layer 22 as shown in the figure, see also figure 2 and col. 9, lines 30-40) and conducts electric currents in and out of the electronic component; n-th conductive layer is an external connecting layer for connecting external connecting terminals (24) which conduct electric current in and out of the printed wiring board; a second to (n-1)-th conductive layers are current transmitting layers for transmitting internal currents of the printed wiring board; and a surface of the n-th conductive layer is covered with an n-th and outermost insulating layer with external connecting terminals being exposed. Takenouchi does not specifically state that a central insulating layer of the odd number of insulating layers prevents warping from occurring in the printed wiring [claim 1]. However, Takenouchi does teach that the insulating layers are comprised of a thermosetting film (see col. 9,

lines 60-65). It is well known in the art to comprise thermosetting films of glass reinforced thermosetting films to add structural rigidity to the device as evidenced by Ishii (see col. 7, lines 5-20). Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to use a glass reinforced prepreg layer as the thermosetting film in the invention of Takenouchi as is well known in the art and evidenced by Ishii. The motivation for doing so would have been to provide structurally rigidity to the device to avoid damaging the circuit patterns when the semiconductor device is mounted. Additionally, the modified invention of Takenouchi teaches, wherein the external connecting terminals are solder balls [claim 2].

Similarly, regarding claim 10, Takenouchi discloses the claimed invention as described above except Takenouchi does not specifically state that the films are mare of glass fiber reinforced resin. However, Takenouchi does teach that the insulating layers are comprised of a thermosetting film (see col. 9, lines 60-65) [claim 10]. It is well known in the art to comprise thermosetting films of glass reinforced thermosetting films to add structural rigidity to the device as evidenced by Ishii (see col. 7, lines 5-20). Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to use a glass reinforced prepreg layer as the thermosetting film in the invention of Takenouchi as is well known in the art and evidenced by Ishii. The motivation for doing so would have been to provide structurally rigidity to the device to avoid damaging the circuit patterns when the semiconductor device is mounted.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over US 5,010,641 (Sisler) in view of US 4,180,608 (Del).

Sisler discloses, referring to figure 2, a printed wiring board comprising an internal insulating substrate (18) having a conductor circuit (17) formed on a surface thereof an internal insulating layer (14, 16) laminated on the surface of the internal insulating substrate, and an external insulating layer (12) laminated on a surface of the internal insulating layer, the internal insulating layer and the external insulating layer having an internal conductor circuit (13) and an external conductor (11) circuit respectively: wherein the internal insulating layer comprises two or more internal insulating layers of glass cloth-reinforced prepreg (see col. 3, lines 40-50). Sisler does not specifically state that the prepreg contains 30 to 70% by weight of glass cloth. However, it is well known in the art to comprise prepreg sheets having 30-70% by weight of glass cloth as evidenced by Del (see col. 1, lines 30-40). Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to comprise the sheets in the invention of Sisler of 30-70% glass cloth as is well known in the art and evidenced by Del. The motivation for doing so would have been to provide the layers with the necessary dielectric properties, thus avoiding unwanted shorting and creating a more reliable device (see Del. col. 1, lines 30-40).

Claims 15 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5,541,368 (Swamy) in view of US 5,734,560 (Kamperman).

Swamy discloses, referring to figure 2a, a printed wiring board comprising an interconnecting through hole (44) penetrating an insulating substrate, an annular pad (54) disposed along a peripheral edge of one opening of the interconnecting through hole so as not to cover the opening: a second pad on the other opening of the interconnecting through hole and a conductor circuit (see col. 7, lines 5-20) connected to the pad; wherein the annular pad and the second pad are electrically connected to each other by a metal plating film (50) covering a wall of the interconnecting through hole; and a solder ball (24) for external connection is located onto the surface of the annular pad at a position offset from the interconnecting through hole. Swamy does not specifically state that the second pad is a covering pad covering the opening in the through hole [claim 15]. However, it is well known in the art to comprise pads connect to through holes as covering pads which cover the through holes as evidenced by Kamperman (see figure 2, and col. 2, lines 55-65). Therefore it would have been obvious to one having ordinary skill in the art at the time of invention to use a covering pad as the second pad in the invention of Swamy as is well known in the art and evidenced by Kamperman. The motivation for doing so would have been to prevent unwanted material from entering the via (Kamperman col. 4, lines 25-35). Additionally, the modified invention of Swamy teaches, wherein the surface of the insulating substrate is covered with a solder resist (56) [claim 18].

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeremy C. Norris whose telephone number is 571-272-1932. The examiner can normally be reached on Monday - Friday, 9:30 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JCSN

RANDY GIBSON
PRIMARY EXAMINER